A 3-V 230-MHz CMOS Decimation Subsampler

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***Abstract*—The use of subsampling for frequency downconversion and related tradeoffs in radio receivers are discussed. It is found that using the highest possible sampling frequency both relaxes anti-alias filtering requirements and reduces the effect of clock jitter. However, high-speed switched-capacitor circuits are difficult to design and they are typically power consuming. A switched-capacitor decimation sampler is proposed as a way to achieve more optimal sampling frequencies both at the input and the output of the sampler.**

The design and experimental results of a 3-V 230-MHz CMOS decimation subsampler are presented. The sampler achieves an input referred noise density of 44 nV/$\sqrt{\text{Hz}}$, an IIP_3 of +19.5 dBV, and a −52-dBc worst mixing product from clock skew with a 200-MHz input.

***Index Terms*—Frequency downconversion, IF-receiver, subsampling.**

I. Introduction

SUBSAMPLING has recently gained a lot of attention as a frequency downconversion method for radio receivers [1]–[6]. The main motivation behind this is the need to go for more digital implementation by pushing the analog-to-digital conversion (ADC) boundary higher in frequency. This would enable the increasing of the product integration level and consequently decrease the physical size, improve the reliability and reduce the manufacturing cost. The ultimate goal is of course direct digitization from RF which would eliminate all other analog components from the receive path except the RF filter and the LNA. This kind of approach, often dubbed as the software radio, would offer a high degree of programmability and thus lend itself very naturally to multistandard operation. Unfortunately, the required ADC dynamic range and sampling frequency are extremely high. For example, an ADC suitable for a Global System for Mobile Communications (GSM) software radio would need to digitize a 900-MHz signal with at least 16 bits of resolution [7], which is not feasible with the existing technology.

Digitization from an intermediate frequency rather than RF is much more viable, because of the relaxed ADC sampling aperture and anti-alias filtering requirements. In a base station application it might be desirable to perform a wideband ADC of all received channels and then process them in the digital domain.

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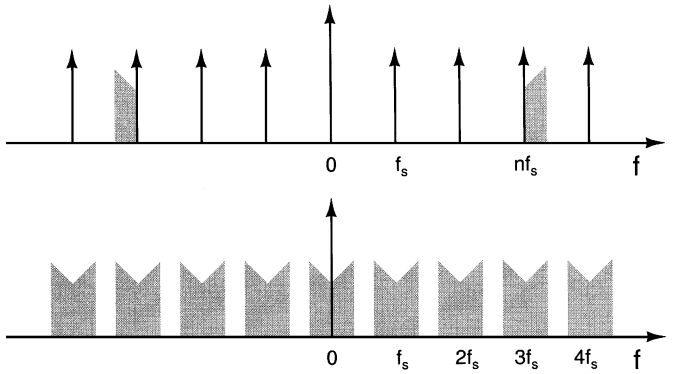


Fig. 1. Subsampling downconversion.

In such a case, the final frequency downconversion to the baseband is performed digitally and the analog IF mixing is eliminated. However, a high resolution wideband ADC has a prohibitively high power consumption for battery operated handsets. As an alternative, subsampling can be used in combination with a noise shaping ADC ($\Delta\Sigma$-modulator) to digitize a single channel directly from IF. Noise shaping converters combine high sampling rate with a high resolution over a narrow band in a very power efficient manner which makes them well suited for the ADC of relatively narrow radio channels. In a superheterodyne receiver, where the IFs are fixed, a subsampling downconverter can be clocked directly from a fixed crystal oscillator thus relaxing the frequency synthesis of the receiver. Furthermore, a subsampler can be readily combined with the input of an A/D-converter eliminating continuous-time IF mixers altogether. Assuming sufficiently wideband analog filtering, IF ADC still allows for notable flexibility to be implemented digitally.

The nonidealities and tradeoffs associated with a subsampler in a radio receiver are discussed in more detail in Section II. The proposed decimation sampler technique and the design of a prototype circuit are discussed in Sections III and IV, respectively. Finally, the experimental results of a 230-MHz decimation subsampler are presented in Section V.

II. Subsampling Downconversion

Normally, a continuous-time input to a discrete-time analog system is band limited below the Nyquist frequency $f_S/2$ to prevent higher frequency signals from aliasing on top of the low frequency desired signal. If the signal band is in fact above the Nyquist frequency, it can be downconverted by allowing it to alias below the Nyquist frequency in the sampling process (Fig. 1). However, in this case the input must be bandpass filtered to ensure that the Nyquist criterion is not violated, exactly in the same way as with a baseband signal.

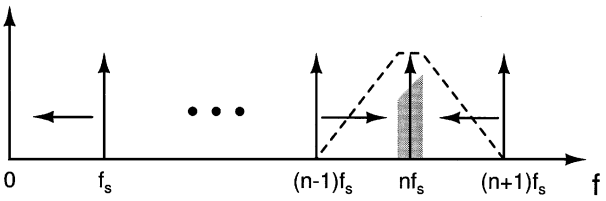


Fig. 2. Tradeoff between sampling frequency and anti-alias filtering.

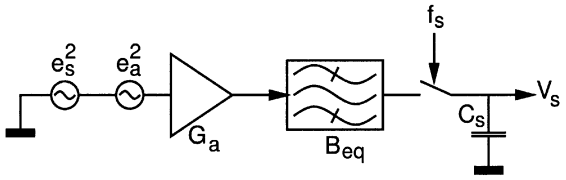


Fig. 3. Model for wideband noise aliasing in a subsampling receiver.

The alias frequencies which can be downconverted to an intermediate frequency $f_{\rm IF}$ by subsampling are given by

$$f_{\rm alias} = nf_S \pm f_{\rm IF} \tag{1}$$

where n is an integer larger or equal to one and $f_{\rm IF}$ is limited below the Nyquist frequency. As a special case of (1) all harmonics of the sampling frequency are converted to dc. In a subsampler the clock signal, which is used to perform the downconversion, can be considered to be the local oscillator (LO) signal. The most important consequence of (1) is that the LO does not have to be separated from the input frequency by the next IF, which is the case with conventional mixing, but it can be at some lower frequency. At the radio architecture level, frequency synthesis is simplified considerably because one LO signal can be obtained directly from a relatively low frequency crystal oscillator which is necessary anyway as a frequency reference.

A. Anti-Alias Filtering

The flexibility in the LO frequency selection with subsampling downconversion does not come for free. The main drawback is that the desired signal has a large number of unwanted alias frequencies which must be filtered prior to sampling. Furthermore, decreasing the LO frequency has the effect of moving the unwanted alias frequencies closer to the desired signal which makes them harder to attenuate by filtering (Fig. 2). It follows that the anti-alias filtering is easiest to realize when the LO frequency is placed as high as possible. For a zero IF this means that the LO is selected to coincide with the center frequency f_c of the input signal band. In general, the highest possible LO for subsampling downconversion is given by $f_c + f_{\rm IF}$.

The input referred noise power density of a subsampling downconverter is typically high due to the kT/C-noise. Consequently, a receiver must have sufficient amplification before subsampling to reduce its effect on the system noise figure. Unfortunately, any wideband noise power originating from the preceeding amplifiers will alias below the Nyquist frequency and degrade the receiver noise figure. Let us consider a simple model of a receiver front-end (Fig. 3). The source and preamplifier (or LNA) noise power densities are referred to the input and denoted by e_s^2 and e_a^2. The preamplifier has a voltage gain of G_a and the anti-alias filter an equivalent noise bandwidth of $B_{\rm eq}$. Then the input referred noise power density is given by

$$e_{\rm eq}^2 = \frac{B_{eq}}{f_N}\left(e_s^2 + e_a^2\right) + \frac{e_0^2}{f_N G_a^2} \tag{2}$$

where e_0^2 is the input referred noise power density of the subsampler. Equation (2) demonstrates a very important property of subsampling. The noise power density originating from the source and the circuitry before the sampler will be amplified by the ratio between the equivalent noise bandwidth seen at the sampler input and the Nyquist frequency. Furthermore, the gain of the receiver front-end cannot reduce this effect in any way. As the sampling degrades the noise figure of the preamplifier directly, it is absolutely necessary that the Nyquist frequency f_N of the sampler exceeds the equivalent noise bandwidth $B_{\rm eq}$ seen at the amplifier output. The situation with conventional mixers is not entirely different. In a superheterodyne receiver an image filter is almost always used to eliminate the noise at the image frequency which would otherwise degrade the noise figure of the LNA by 3 dB.

The high selectivity requirement for anti-alias filtering is one of the reasons prohibiting subsampling from RF in a radio receiver. The preselect filter would have to provide stopband attenuation in the order of 80–100 dB at a relatively small frequency offset from the carrier. The existing RF filters used for preselection and image rejection have stop-band attenuations in the order of 20–40 dB which is clearly insufficient for anti-aliasing.

B. Clock Oscillator

Timing uncertainty (or jitter) in the sampling clock results in amplitude noise which is directly proportional to both input signal amplitude and frequency. For low signal levels the jitter has no impact on the signal to noise ratio which is typically limited by thermal and other device noise sources. However, as the signal level is increased, the clock jitter will eventually limit the SNR to a certain maximum [8] given by

$$\mathrm{SNR}_{\max} = \frac{1}{\left(2\pi f_s \sigma_j\right)^2} \tag{3}$$

where σ_j is the rms-value of the sampling jitter.

In digital communication systems the signal is not supposed to be sampled at the zero crossings, but at the time instants where the eye opening of the received data is widest and the detection of the bits is easy. If the signal is sampled at its maxima or minima, the timing jitter will have no first-order effect on the accuracy. However, in a radio receiver the interfering signals, like neighboring channels, may be much larger than the desired signal, so that the assumption of sampling at the derivative zeros is not valid.

In communication systems the quality of the local oscillator signal is more commonly expressed as phase noise power density to carrier ratio $\mathcal{L}(f_m)$ in 1-Hz bandwidth at a given frequency offset f_m rather than time jitter. It can be shown that subsampling has the effect of multiplying $\mathcal{L}(f_m)$ by the ratio

f_c/f_s squared [4]. Then the maximum signal power to noise ratio is given by

$$\mathrm{SNR}_{\max} = \left(\frac{f_s}{f_c}\right)^2 \times \mathrm{SNR}_{\mathrm{clk}} \tag{4}$$

where f_s and f_c are the sampling and carrier frequencies, respectively, and $\mathrm{SNR}_{\mathrm{clk}}$ is the signal to noise ratio of the sampling clock. The reason for the phase noise power being multiplied in this fashion is that a given time deviation at the sampling frequency corresponds to a proportionally larger phase deviation at the carrier frequency.

Although, the local oscillator phase noise requirement is, according to (4), more stringent for subsampling than mixing downconversion, a low phase noise is easier to realize at a lower frequency. The oscillator phase noise $\mathcal{L}(f_m)$ in the $1/f^2$-region is inversely proportional to the ratio f_{osc}/Q squared [9] suggesting that, due to the lower frequency and higher Q values obtainable by crystal resonators, a given phase noise power specification should be easier to meet by subsampling. However, the noise floor of the clock oscillator and the subsequent buffer amplifier is not dependent on the oscillation frequency and will eventually dominate the phase noise for lower oscillation frequencies[10]. When this is the case the signal SNR can be improved by digitally filtering the out-of-band noise. Assuming brickwall filtering and white noise, the maximum signal-to-noise ratio is given by

$$\mathrm{SNR}_{\max} = \left(\frac{f_s}{f_c}\right)^2 \times \mathrm{SNR}_{\mathrm{clk}} \times \mathrm{OSR} \tag{5}$$

where OSR is the ratio between the Nyquist frequency and the signal bandwidth. From (5) it can be deduced that using a high sampling frequency decreases the sensitivity to clock jitter as long as it is dominated by the noise floor of the oscillator and buffer amplifier. Increasing the sampling frequency to the region where the sampling clock phase noise is dominated by the oscillator $1/f^2$-noise will provide no improvement.

C. Sampling Aperture

Naturally, a real sampler cannot capture and downconvert signals from infinitely high input frequencies. In order to do that, the sampler would need to have an infinite tracking bandwidth and it would have to move instantly from tracking to hold. In the time domain sampling can be described as a function which takes a weighted average of the input signal [11]. Assuming that a sampler is tracking the signal in steady state and that a sample acquisition is completed at $t = 0$, the output signal is given by

$$v_o(t=0) = \int_{-\infty}^{0} SF(\tau) v_{\mathrm{in}}(\tau) d\tau \tag{6}$$

where $SF(\tau)$ is the sampling function. Let us denote the hold capacitor by C_s and assume that the sampling switch conductance changes linearly from an initial value of g_s to zero during the time interval $-t_f$ and 0. Then the sampling function can be found as (Appendix)

$$\begin{cases} SF(\tau) = \dfrac{g_s}{C_s} e^{g_s/C_s(t_f/2+\tau)}, & \tau < -t_f \\ SF(\tau) = -\dfrac{g_s}{C_s}\dfrac{\tau}{t_f} e^{-g_s/2C_s t_f \tau^2}, & -t_f \le \tau < 0. \end{cases} \tag{7}$$

The frequency response of a sampler can be obtained by Fourier transforming its sampling function [11]. Alternatively, the width of the sampling function in the time domain can be used as a measure of the sampler speed.

Let us define the sampling aperture as the width of a rectangular sampling function with the height equal to the maximum of the actual sampling function $SF(\tau)$ (Appendix). Then the sampling aperture in two different cases is given by

$$a_t = \begin{cases} \sqrt{\tau_s t_f e}, & t_f > \dfrac{C_s}{g_s} \\ \tau_s e^{1/2t_f/\tau_s}, & t_f \le \dfrac{C_s}{g_s} \end{cases} \tag{8}$$

where τ_s is the switch *RC*-time constant C_s/g_s. Equation (8) suggests that the aperture time of a sampler is proportional to the geometric average of the *RC*-time constant of the sampler τ_s and the switch opening time t_f when the switch opening time is longer than the sampler *RC*-time constant. If t_f is shorter than τ_s, then the sampler will be dominated by the tracking mode bandwidth and the sampling aperture will approach the sampler *RC*-time constant. Assuming $t_f \ll \tau_s$, the aperture time can be approximated by

$$a_t \approx \tau_s + \frac{t_f}{2}. \tag{9}$$

Generally, the sampling aperture is signal dependent giving rise to harmonic distortion if the input contains high frequency signal components [12]. In a radio receiver the sampler should be designed to have a sufficiently wide bandwidth to pass, not only the desired channel, but also higher frequency interferers unattenuated. Otherwise, intermodulation distortion may corrupt the desired channel.

Some circuit techniques can be utilized to reduce the distortion from a signal dependent sampling aperture. Bottom-plate sampling eliminates signal dependency from the sampling instant (t_f becomes constant) although at a price of higher series resistance on the signal path. The signal dependency of the top-plate switch on-resistance can be reduced (τ_s becomes constant) by ac-coupling the switch-transistor gate to the input and thus generating a constant gate to channel voltage [13].

D. System Architectures

The system architectures for a subsampling receiver can be roughly divided into two categories. If the subsampled signal is downconverted to a nonzero IF, a wideband ADC [14] or a bandpass $\Delta\Sigma$-modulator [15], [16] is used for the digitization of the signal, and the demodulation is performed in the digital domain [Fig. 4(a)]. Alternatively, the input signal can be downconverted directly to dc by using two subsamplers with a 90° phase shift [17] in order to resolve both the positive and negative sides of the channel spectrum [Fig. 4(b)]. In this case the ADC can be performed with two lowpass $\Delta\Sigma$-modulators, which are much easier to realize with a high performance than bandpass $\Delta\Sigma$-modulators. Furthermore, the sampling frequencies in the in-phase (I) and quadrature-phase (Q) signal branches can be halved compared to a case of nonzero IF. This is because the signal spectrum is centered at the dc and it can extend from $-f_N$ to f_N without aliasing. Of course, the overall sampling

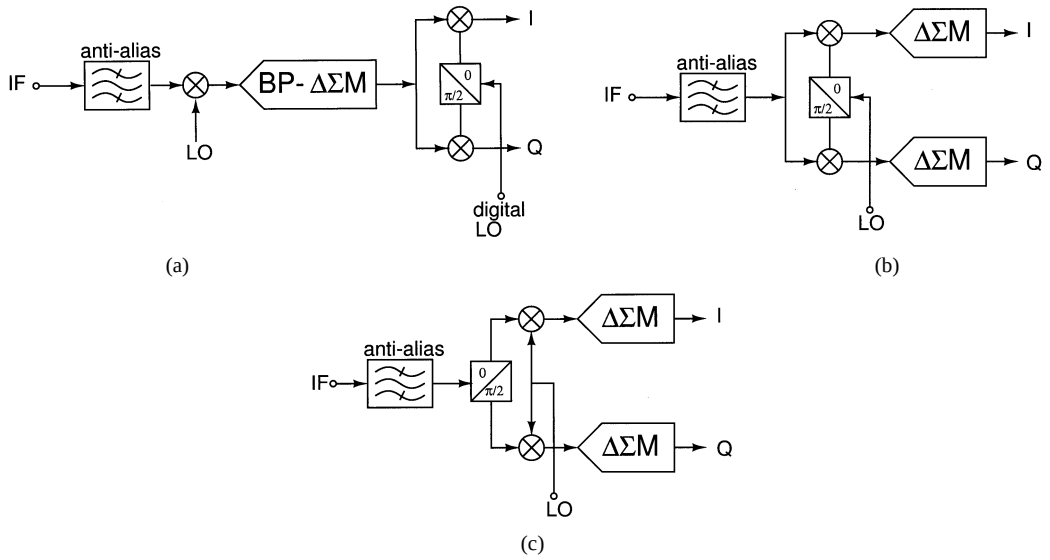


Fig. 4. System configurations for a subsampling IF-receiver.

frequency can be defined as the sum of the I and Q sampling clock frequencies, in which case there is no real difference and (2) still holds.

In the case of separate I and Q subsamplers, the generation of the required two clock signals with an accurate phase difference is not totally trivial. This is because the clock signals must be in quadrature phases at the input frequency and not at the sampling frequency. It follows that, the clock signals should be separated by

$$\Delta\phi = \frac{f_s}{f_c}\frac{\pi}{2} \tag{10}$$

where f_s and f_c are the sampling and input center frequencies, respectively.

For continuous-time I/Q mixers, the local oscillator phases are often obtained by dividing a higher frequency clock [18] or with a *RC-CR* network. If the I and Q clocks are derived by division, (10) implies that, the frequency of the required clock depends only on the input center frequency and not at all on the actual sampling frequency. Consequently, lowering the sampling frequency does not, in this case, relax the frequency synthesis. The *RC–CR* network, on the other hand, can only be used to derive a 90° phase difference, so its applicability is limited to the case $f_s = f_c$.

As a third alternative, the input signals could be phase shifted instead of the sampling clocks [Fig. 4(c)]. Then a simple *RC–CR* network can be used. However, it may be difficult to obtain a sufficiently good amplitude matching between the I and Q signal paths, because, unlike the local oscillator, the actual signals cannot be limited before the channel selection filtering has been performed.

III. Decimation Sampling

There are several reasons why it is advantageous to sample at a high frequency, as discussed in Section II. The anti-alias filtering is relaxed, input noise aliasing is reduced and the effect of jitter is mitigated due to the increase in the oversampling ratio.

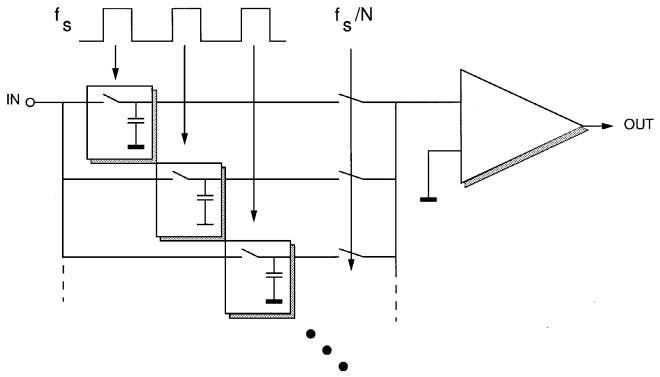


Fig. 5. Conceptual diagram of the decimation sampler.

In principle, the sampling frequency of a MOS-sampler can be very high as it is limited foremost by the clock driver. Unfortunately, it is not sufficient that a sample is acquired, but it has to be buffered out and processed further by active analog circuitry which imposes much more stringent limitations on the sampling frequency. It is not only difficult to design and implement a very high speed buffer amplifier, but it is often also undesirable because of the inherently high power consumption involved.

A. Decimation Sampling Technique

The rectriction on the sampling frequency can be removed by placing several MOS-samplers in parallel, running them with a high clock frequency and then buffering them out simultaneously at a reduced frequency (Fig. 5) [19]. The result is that, if N samples are acquired to different hold capacitors and then connected in parallel to be buffered out, the sampling frequency is N times higher than the clock frequency of the buffer amplifier and the subsequent circuitry.

While the N samples are being buffered, the acquisition of the next set of N samples must be in progress. Therefore, some redundancy in the number of samplers is necessary or alternatively the charge transfer from the hold capacitors to the buffer has to take place instantaneously. If we asume 50% of the time is used for buffering, a minimum of $3N/2$ samplers are needed

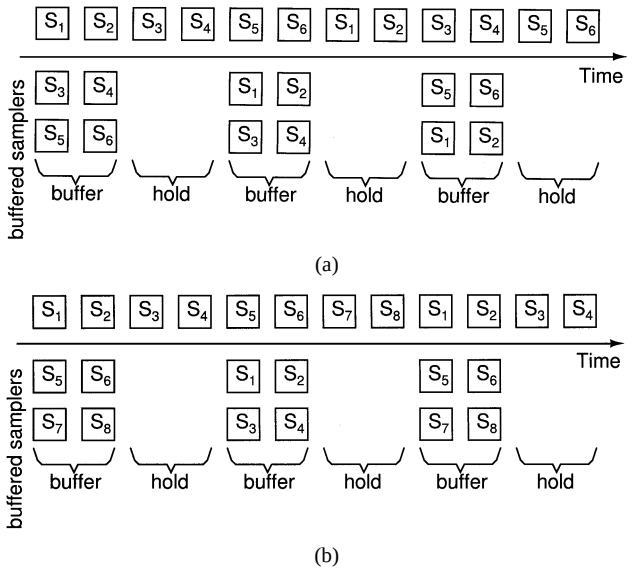


Fig. 6. (a) Sampling and buffering order with a minimum number of $3N/2$ hold capacitors. (b) With $2N$ hold capacitors ($N = 4$).

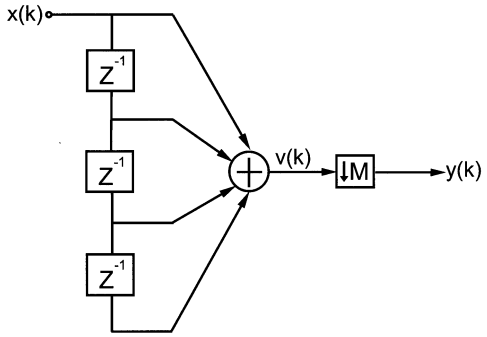


Fig. 7. z-domain SFG representation of a decimation sampler with $N = 4$.

because N hold capacitors are connected at the same time to the output buffer and $N/2$ samples still have to be acquired during that time. Implementing the sampler with the minimum number of hold capacitors makes the clock generation circuitry unnecessarily complicated because there are three different hold capacitor combinations that need to be buffered out [Fig. 6(a)]. The clock generation can be somewhat simplified by using $2N$ hold capacitors, because then there are two fixed sets of N hold capacitors which are buffered out in turn [Fig. 6(b)].

A signal processing block reducing the sample rate performs a decimation operation, which can be considered as a discrete time equivalent to subsampling. Consequently, the spectrum of the decimated signal will fold in the same way as the spectrum of a subsampled signal potentially corrupting it. A decimation sampler with $N = 4$ can be represented with a z-domain signal flow graph in Fig. 7. The output of the sampler $v(k)$ in the general case is formed as the sum of N consecutive samples

$$v(k) = \Sigma_{i=0}^{N-1} x(k-i). \tag{11}$$

The z-domain transfer function $V(z)/H(z)$ is given by

$$\frac{V(z)}{H(z)} = \Sigma_{i=1}^{N} z^{1-i} \tag{12}$$

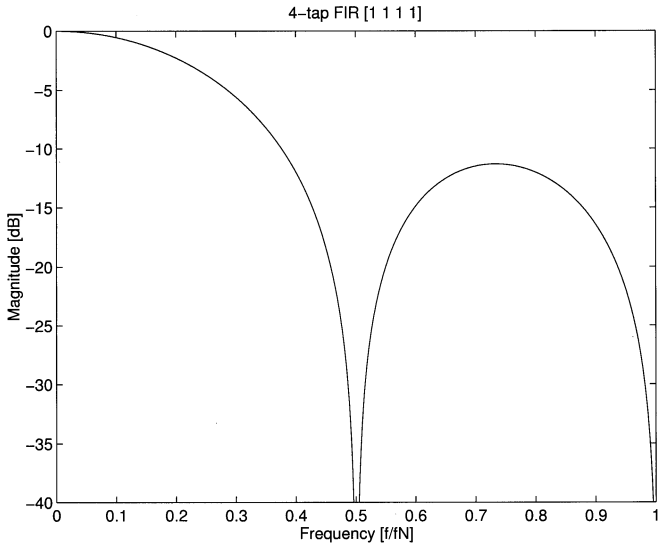


Fig. 8. Transfer function $V(z)/X(z)$ of the four-tap FIR with equal tap weights. The transmission zeros are placed so that no aliasing to dc occurs when signal is decimated by 4.

which is a finite impulse response (FIR) filter with N equally weighted taps. The magnitude response of such a filter is plotted in Fig. 8 for $N = 4$. The decimation cause the original spectrum to fold inside the Nyquist frequency of the reduced sample rate which is N times lower. From Fig. 8. we may note that the zeros of the FIR are located so that no power is aliased to dc in the decimation process. This means that as long as the band of interest is narrow compared to the undecimated Nyquist frequency, the sampler will, looking from the input, behave as if it had N times higher sampling rate than the output buffer. Consequently, the anti-alias filtering is relaxed and the effect of wideband noise aliasing and clock jitter are reduced according to the N times higher input frequency.

None of the listed positive effects depend on the size of a unit hold capacitor (denoted from here on as C_u). If we select C_u to be equal to C_h/N, the total load capacitance and therefore also the power consumption of the buffer amplifier are identical to a lower sampling frequency design with a hold capacitor of C_h.

Assuming the thermal noise power n_u^2 from one unit hold capacitor is kT/C_u, the corresponding noise charge in N unit capacitors is given by

$$Q_n = \sqrt{NkTC_u}. \tag{13}$$

The thermal noise power in the N combined capacitors is

$$n_0^2 = \left(\frac{Q_n}{N_{C_u}}\right)^2 = \frac{kT}{C_h} \tag{14}$$

which is the same as if sampling had been carried out at once into one large hold capacitor C_h. However, the Nyquist frequency is also lower and the power spectral density expectedly remains unchanged along with the power consumption.

Naturally, the clock generation is more complicated and will consume extra power. However, let us assume that most of the power in the clock generation circuitry is consumed by the sampling switch drivers which is justified in a subsampler by the tight sampling aperture requirement. In order to keep

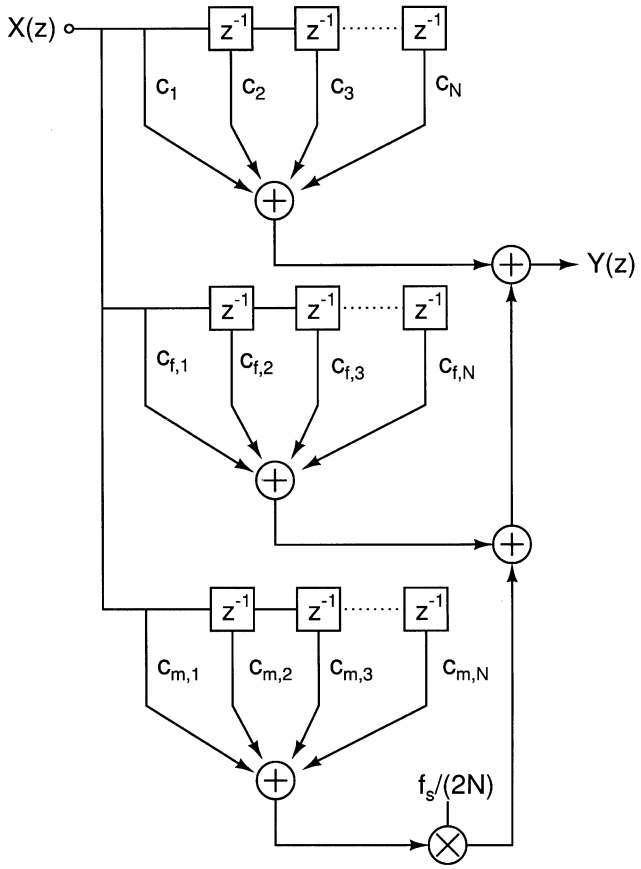


Fig. 9. Effect of mismatch in a decimation sampler.

the *RC*-time constant of a unit sampler the same as that of a conventional MOS-sampler, the width of the switches can be scaled down by N. Then the switch drivers can also be scaled down and there is no first-order power penalty.

B. Path Mismatch

In analog systems with parallel paths, the matching between the paths is always a concern [20]. Here the discussion is limited to the case of two fixed sampler sets with N unit samplers in each. In the case of two signal paths, the gain mismatch will have the effect of a weakly modulating signal at the decimated Nyquist frequency and its multiples. The frequencies closest to the desired signal, which will mix to dc are given by

$$f_{\text{mix}} = \frac{f_c \pm f_s}{(2N)}. \tag{15}$$

Multiple analog signal paths are also bound to have different delays. The delay skew will appear in a same manner as the gain mismatch, except that its effect is frequency dependent. Obviously, variation in the path delay has no effect, when a dc signal is sampled. As the signal frequency is increased the path delay variation produces an error with an increasing amplitude making it a serious problem for high frequency samplers.

The mismatches between capacitors will produce coefficient errors also inside a single capacitor set. The gain variation between the two sets and the inter-set mismatch can be separated by dividing the signal path into three components (Fig. 9). The ideal FIR coefficients c_i, a fixed error FIR which represents the fixed error in the transfer function and a gain mismatch FIR, which represents the mismatch between the sampler sets. Let the nonideal coefficients of the two FIRs be denoted as $c_{\text{p1,i}}$ and $c_{\text{p2,i}}$. Then the coefficients of the fixed error and gain mismatch FIRs are given by

$$\begin{aligned} c_{\text{f,i}} &= c_i - \frac{1}{2}(c_{\text{p1,i}} + c_{\text{p2,i}}) \\ c_{\text{m,i}} &= \frac{1}{2}(c_{\text{p1,i}} - c_{\text{p2,i}}). \end{aligned} \tag{16}$$

The coefficients in both fixed error and gain mismatch FIRs are random and thus the exact frequency characteristic will vary from sample to sample. The fixed error FIR will have the effect of passing signals which are located at the transmission zeros of the ideal filter. As a consequence, some power from the alias frequencies will be converted down to the baseband in the decimation.

In practice, a subsampler is preceded with an anti-alias filter which must have large attenuation at frequency offsets f_S from the input center frequency. Then it is likely, that the anti-alias filter will provide substantial attenuation already earlier at the frequency offsets of $f_S/(2N)$ and f_S/N, which will help to suppress the effect of parasitic mixing results from analog nonidealities.

IV. Circuit Design

A switched capacitor decimation subsampler was implemented in a 0.5-μm CMOS process to demonstrate the feasibility of the proposed technique. The decimation ratio was selected to be four, which reduces the clock rate considerably, while keeping the circuit complexity and anti-alias filtering requirements at a reasonable level. An output buffer utilizing a unity-gain feedback configuration was used to obtain good linearity and insensitivity to parasitic capacitances. Alternatively, the SC-samplers could be interfaced directly to any switched-capacitor signal processing block such as a channel selection filter or A/D converter.

A. Parallel Sampler

Although a minimum number of six unit samplers would have been sufficient for a decimation ratio of four, it was decided to use eight samplers instead in order to simplify the clock signal generation and to reduce the number of switches. An overall schematic of the sampler excluding the clock generation is shown in Fig. 10. The samplers are divided into two sets which are buffered out successively during the clock phases A and B. The buffer holds the previous output sample for 50% of the time, so that two input samples can be taken then and the other two while the previously sampled capacitor set is being buffered.

The unit samplers perform the sampling with bottom plate switches to reduce the effect of sampling aperture distortion and switch charge injection. The circuit is fully differential to reduce the even-order distortion components and the bottom plate switches are combined to reduce the series resistance and thus the sampling aperture [3]. The input common-mode level was

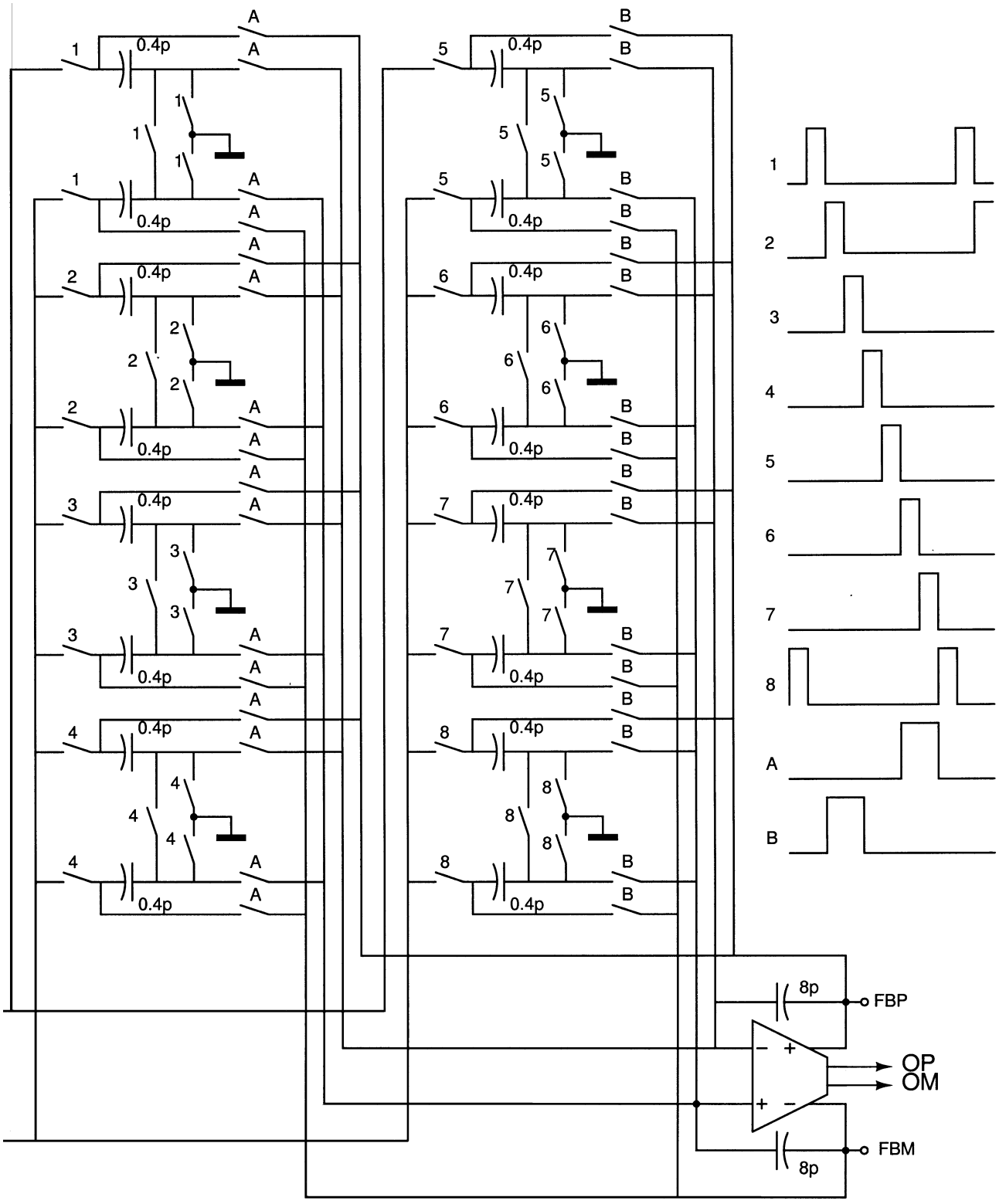


Fig. 10. Schematic of the implemented decimation subsampler.

selected to be 700 mV above the V_{SS} to maximize the gate to channel voltage which improves the linearity at high input frequencies. Only NMOS switches were used as it would have been difficult to properly conductance-scale a CMOS switch at the low common-mode level of 700 mV. Furthermore, the tracking linearity would have been degraded by sharp changes in the switch on-resistance introduced by the PMOS turning ON and OFF.

The hold capacitors of the unit samplers were selected to be 0.4 pF. The size was mainly set by a tradeoff between thermal noise and switch driver requirements. Large hold capacitors would have led to wide switches and increased switching noise

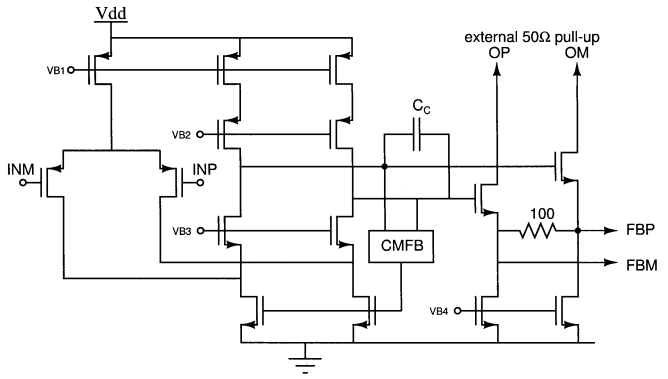


Fig. 11. Buffer amplifier.

in the digital supplies and the substrate. Also, distributing the sampling clock with a low skew is more difficult if the samplers are widely separated from each other in the layout.

B. Buffer

The sampler buffer is configured as a unity-gain feedback amplifier. A fixed feedback capacitor introducing a low frequency pole was added to establish a feedback path for the operational amplifier at all times and to improve the out-of-band linearity of the sampler. Let the fixed feedback capacitor be C_f and the combination of the parallel hold capacitors C_h, then the buffer transfer function is given by

$$H_B(z) = \frac{\frac{C_h}{C_f}}{\frac{C_h}{C_f} + 1 - z^{-1}}. \tag{17}$$

The pole was set to a low frequency by selecting a feedback capacitor of 8 pF. This makes the buffer sensitive to absolute values of the hold capacitors but it also relaxes the amplifier settling requirements and, therefore, improves the out-of-band linearity of the sampler. It should be noted that, while holding the signal, the feedback capacitor also holds the thermal noise of the switches. This has the effect of increasing the switch thermal noise contribution from the sampling capacitors to $2kT/C_h$.

The unity-gain SC-amplifier could be used also without the fixed feedback capacitors. Then the gain mismatch between the two paths would be cancelled to first-order, because the sampled voltage is buffered directly and there is no charge transfer involved. However, this would have complicated the circuit design somewhat and provided no improvement against the clock skew which can be expected to be a more serious problem at high input frequencies.

The buffer was designed to drive a 50-Ω load to facilitate testing. In a more integrated system the hold amplifier is followed by other switched capacitor circuitry and it is not necessary for the buffer to be capable of driving a low impedance load. A two-stage opamp with a current output from the second stage [1] was used to achieve reasonable voltage gain and phase margin (Fig. 11). The first stage was a folded cascode OTA with PMOS inputs for low $1/f$ noise. Also, the low common-mode level favored a PMOS type input differential pair. The simulated characteristics of the OTA are summarized in Table I.

TABLE I
SIMULATED CHARACTERISTICS OF THE BUFFER AMPLIFIER

GBW	100MHz
SR	125V/μs
ϕ_m	68°
A_{DC}	62dB
Diff. output range	$1.2V_{pp}$
Voltage supply	3V
Current consumption	10mA

C. Clock Generation

The sampling clock generation was performed with an 8-bit shift register connected in a loop (Fig. 12). This approach has both low power consumption and high-speed capability, because only two flip-flops have a state transition at a time and there is no traversal of logic signals except at clock edges. The shift register does not drive the sampling switches, but it merely provides enable signals enabling one of the switch drivers at a time to perform the sampling. This relaxes the speed requirements of the flip-flops and reduces the clock skew between different samplers as all sampling signals are derived from the same master clock. The layout of the clock distribution was also designed so that there are equally long clock-lines to all drivers from the input clock buffer. Similarly, the input network was drawn as a tree with equally long paths to all samplers.

The sampling clock skew can be further reduced by placing an enable switch in series with the actual sampling switch [21]. This eliminates the delay differences between clock drivers, but adds some series resistance to the high frequency signal path.

V. EXPERIMENTAL RESULTS

The implemented decimation sampler was packaged in a 44-pin CQFP which was directly mounted on a two-level printed circuit test board. Both the analog ground (common-mode level) and the buffer bias current were obtained from external signal sources. The digital and analog supplies were stabilized with 100 nF surface mount capacitors and 1-μF polystyrene capacitors. The bulks of the transistors in digital cells were connected to dedicated power supplies to reduce interference via the conductive CMOS substrate. The bulk supplies were connected to the stabilized main digital supplies on the PCB. The ground plane of the printed circuit board was split to separate analog and digital parts.

The clock signal was obtained from a Rohde & Schwartz SMY01 signal generator except in the jitter measurements where a 50-MHz crystal oscillator was used. The clock input was resistively terminated to 50 Ω on the PCB and dc-decoupled to provide a suitable bias for the input clock buffer.

The differential input signal was generated with a passive balun and the inputs to the PCB were terminated with 50-Ω resistors. The differential to single-ended conversion in the output was performed with an instrumentation amplifier arrangement. It was necessary to use active circuitry in the conversion because of the low output frequency range. The instrumentation amplifier also strongly attenuated the common-mode clock signal present at the differential output.

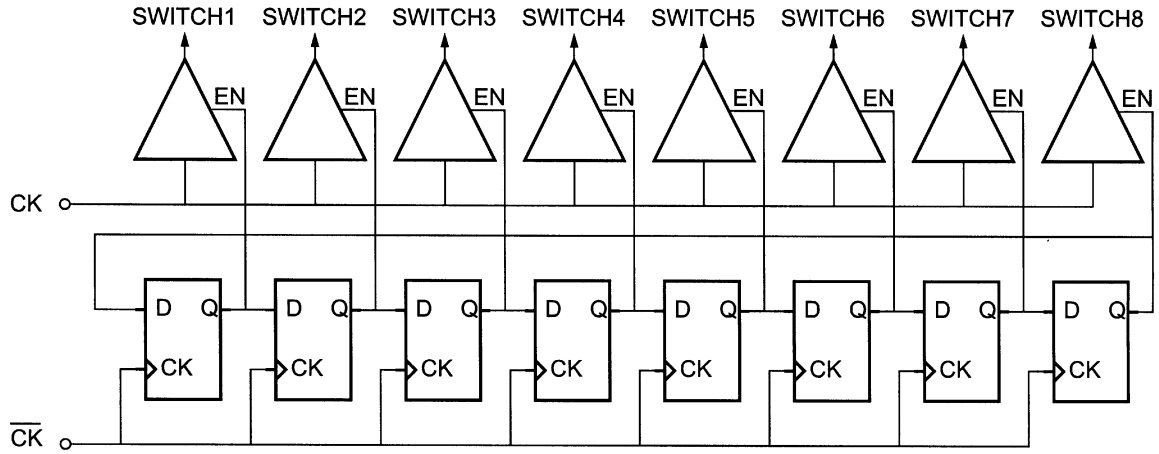


Fig. 12. Eight-phase sampling clock generator.

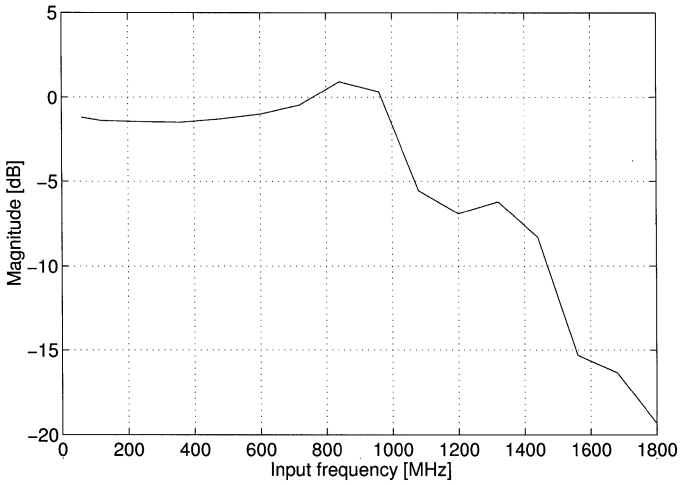
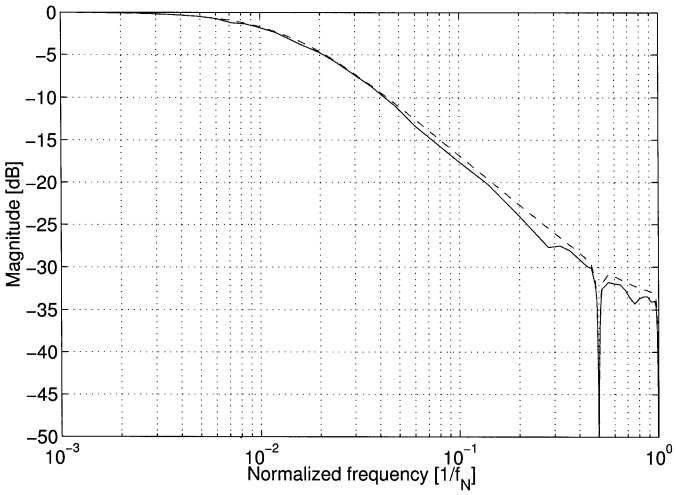


Fig. 13. Measured RF-response.

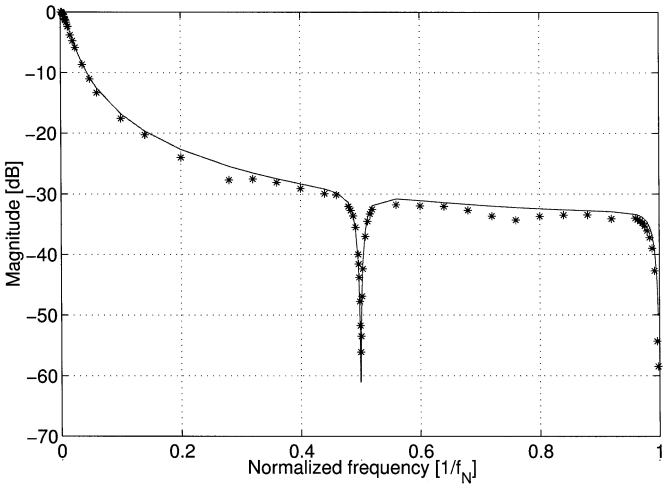
The RF response of the sampler was measured by clocking the sampler at 60 MHz and sweeping the input signal from 60–2040 MHz, so that the signal was always converted to 30 kHz. The measured magnitude response is plotted in Fig. 13. The sampler has a 1.2-dB loss at low frequencies, which is attributed to the output stage 100-Ω resistor deviating from its nominal value. Apart from the small loss, the magnitude response is relatively flat up to 800 MHz after which the magnitude first peaks slightly and then begins to fall rapidly. It is not possible to estimate the sampling aperture of the circuit from this test configuration because the sampler frequency response is masked by the package parasitics. However, it appears that there is no serious bandwidth limitation below 1 GHz.

The IF response was measured by clocking the sampler at 50 MHz and sweeping the input frequency in small steps from 50–75 MHz. The magnitude response to sampler output is a combination of the transfer function of the input sampling network and the output buffer. The buffer is preceded by a decimation so its transfer function undergoes a transformation $z^D \rightarrow z$, where D, the decimation ratio, is 4 in this case. The combined z-domain transfer function is then obtained as

$$H_{\mathrm{IF}}(z) = \frac{1}{4}\frac{1 + z^{-1} + z^{-2} + z^{-3}}{\frac{5}{4} - z^{-4}}. \tag{18}$$



(a)



(b)

Fig. 14. (a) Measured (solid) and theoretical (dashed) IF-response in logarithmic frequency scale. (b) The IF-response in linear scale (to emphasize notches).

The measured IF response is plotted together with the theoretical curve in Fig. 14(a). The 1.2-dB loss of the sampler was subtracted from the measured results to help the comparison with the theoretical response. The experimental results match

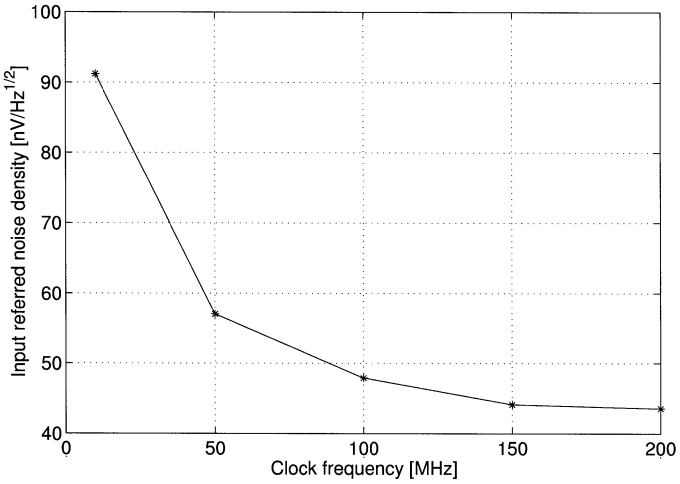


Fig. 15. Measured input referred noise density with no input signal.

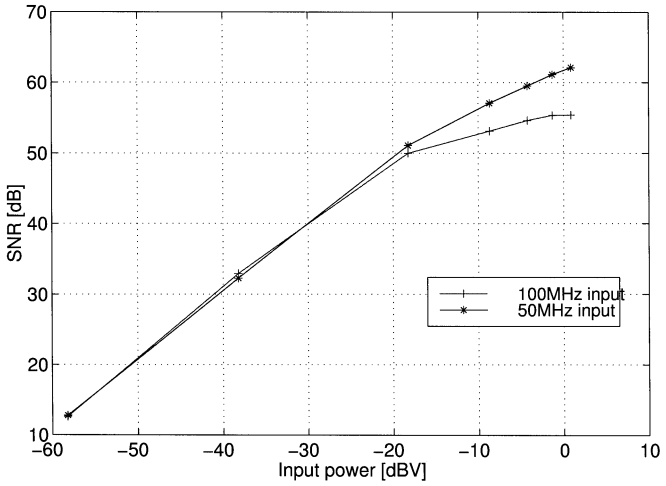


Fig. 16. Measured signal to noise ratio for 53 MHz $(*)$ and 103 $(+)$ input signals.

the theory well apart from two small dips around $f_N/4$ and $3f_N/4$. The same result is plotted in a linear frequency scale to emphasize the transmission zeros, which are important because they reject frequencies that would otherwise alias into the baseband. From Fig. 14(b) it may be noted that around the transmission zeros the results agree very well with the theory and the decimation sampler provides more than 55 dB of rejection for the transmission zero frequencies.

The input referred noise density of the sampler was determined as a function of the clock frequency. The input was terminated with 50-Ω resistors and the output noise was measured with a spectrum analyzer over the band from 10–100 kHz and referred to input by multiplying it with the sampler loss. The obtained input referred noise density (Fig. 15) decreases when the clock frequency is increased and it saturates approximately to 44 nV$/\sqrt{\text{Hz}}$ corresponding to a noise figure of 33.8 dB in a 50-Ω system. The decrease in the noise power spectral density is a consequence of the kT/C-noise being spread over a wider bandwidth. At sufficiently high sampling frequencies the noise density is dominated by the buffer, and is saturated to a certain level.

The jitter of the sampler was measured by clocking it with a 50-MHz crystal and by placing a signal at a 3-MHz offset from the center frequency and sweeping its amplitude. The signal to noise ratio was determined by measuring the output noise power spectral density and multiplying it with the Nyquist frequency. The SNR did not saturate with the 53-MHz input signal and consequently a 103-MHz signal was also applied. The measured signal to noise ratios are plotted in Fig. 16. where the curve corresponding to the 103-MHz input signal saturates to 56 dB. The rms value of the sampling jitter can be calculated from (3) to be 2.5 pS. It was assumed that the jitter from the 50-MHz crystal oscillator was negligible as it had been determined to be less than 1 pS. The signal source jitter was also not accounted for and it may have effected the result.

The linearity of the sampler was determined with an intermodulation distortion test with two interferers placed at 390- and 800-kHz offsets from the center frequency. The third-order distortion product was measured for center frequencies of 50

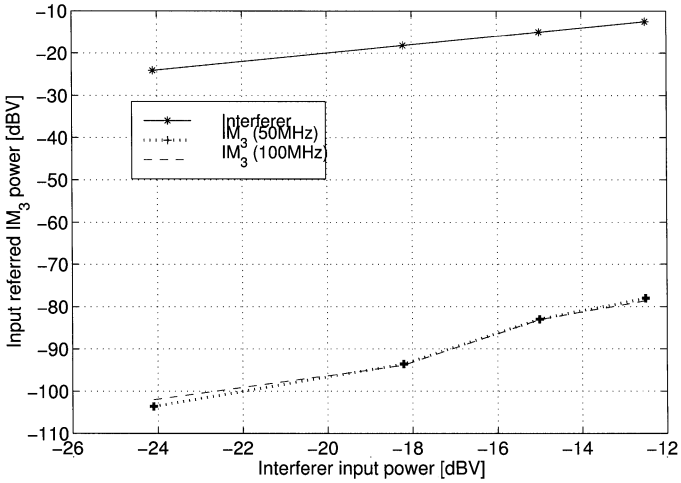


Fig. 17. Measured third-order intermodulation distortion product.

and 100 MHz. The two tones were obtained from Rohde & Schwartz signal generators SMY01 and SMIQ06B and combined with a passive balun. The clock was obtained from a 50-MHz crystal oscillator. The measured IM_3 referred to the input is plotted as a function of input signal to Fig. 17. It is noticed that there is only a short region between -18 and -15 dBV input signals where IM_3 rises with the (ideally) correct slope of three. The IIP_3 was determined from the measured IM_3 at the -18 dBV input level to be $+19.4$ dBV. The linearity did not degrade at all for the higher center frequency of 100 MHz, which suggests that it is, at this level, not dominated by nonlinearities in the actual switched-capacitor samplers.

As discussed in Section III-B, the parallel branches give rise to unwanted mixing products due to gain and delay mismatches between the paths. The only mixing products that could be found in the measurements were downconverted from the frequencies $f_c \pm nf_N/4$, which is predicted by the theoretical model developed in Section III-B. The unwanted mixing products due to path mismatches were measured by clocking the the sampler at 50 MHz and placing an input tone at an offset of $f_N/4$ from different multiples of the clock frequency.

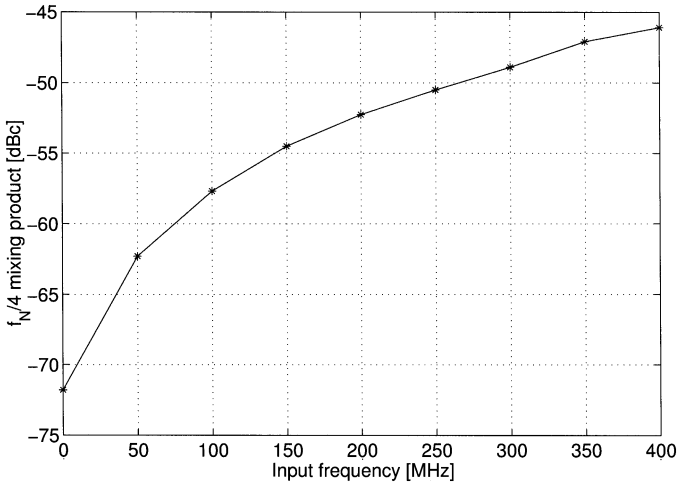


Fig. 18. Measured high-side $f_N/4$ mixing product.

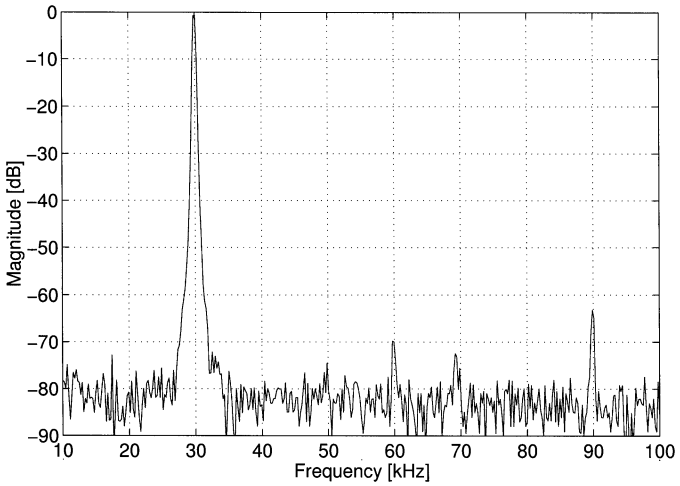


Fig. 19. Measured output for a −12-dBV 230.03-MHz input signal sampled at 230 MHz.

The lowest mixing product from path mismatch, which was 72 dB below the signal, was measured for the input frequency of 6.25 MHz. This suggests that the matching between the capacitors is very good. However, the mixing product rose steadily for higher input center frequencies, which indicates that the mismatch is dominated by the clock skew between the two sampler sets. It was found that the low side mixing product was consistently lower than the mixing product from the high side, although this difference reduced as the input frequency was increased. For input frequencies up to 200 MHz the worst-case unwanted mixing product remains below −52 dBc (Fig. 18). The two fixed sampler sets were laid out in parallel which may have contributed to the clock skew. It is possible that the net clock skew could be reduced by interleaving the sampler sets in the layout.

Since the path mismatches give rise to unwanted frequency conversion that fall on the desired channel, the frequency bands at $f_c \pm nf_N/4$ must be sufficiently attenuated prior to the decimation sampler. However, assuming 40 dB stopband attenuation from the RF preselect filter and front-end matching and −50 dBc unwanted mixing products, yields a combined attenuation of 90 dB for the path mismatch alias frequencies. Consequently, the anti-alias filtering requirements imposed by the path mismatches are very relaxed.

The maximum sampling frequency was measured to be around 230 MHz for the 3-V supply. The analog performance did not degrade significantly when the sampling frequency was increased, which can be attributed to the modest output buffer settling requirements. However, at frequencies above 230 MHz the D flip-flop ring in the clock generator failed to operate correctly. This was slightly unexpected as the clock generator operated correctly up to 700 MHz in the simulations. The measured output spectrum for a −12-dBV 230.03-MHz input signal sampled at 230 MHz is shown in Fig. 19. The third harmonic distortion component is 63 dB below the fundamental and the second harmonic is expectedly slightly lower at −70 dBc.

The measured power consumption was 37 mW at the sampling frequency of 200 MHz. The clock generator consumed roughly 10 mW, which was dominated by the static power consumption in the input clock amplifier. This was confirmed by measuring the current drawn from the digital power supply at lower clock frequencies. A micro photograph of the implemented decimation sampler is shown in Fig. 20. and the performance is summarized in Table II.

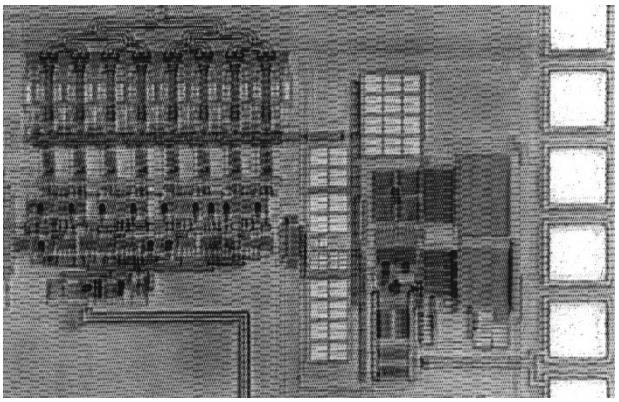


Fig. 20. Microphotograph of the implemented decimation subsampler.

TABLE II
PERFORMANCE SUMMARY OF THE DECIMATION SAMPLER

Technology	0.5μm DPTM CMOS
Sampler area	0.29mm^2
Buffer area	0.25mm^2
Supply voltage	3V
Power consumption	37mW
Maximum sampling frequency	230MHz
Input referred noise density	44nV/√Hz
Samping jitter	2.5pS
IIP3 (100MHz input)	+19.5dBV

VI. CONCLUSION

Using decimation between a sampler and the subsequent circuitry was proposed as a way to achieve more optimal sampling frequencies both at the input and the output of a sampler. The proposed technique can be implemented in an elegant manner with the switched-capacitor technique requiring no modifications to the active analog parts. It was shown that neither area nor power consumption will increase significantly for a constant

thermal noise whereas problems associated with anti-alias filtering, wideband noise aliasing and sampling clock jitter are alleviated.

A 230 MHz switched-capacitor subsampler which decimates the input sampling frequency by four was implemented to experimentally verify the feasibility of the proposed technique. Close matching between theoretical and measured frequency responses was achieved which indicated that the proposed circuit structure can be successfully used to sample and decimate analog signals. Furthermore, unwanted mixing products due to path mismatches were measured to be very low (-72 dBc) for low frequency inputs and moderately low (-52 dBc) even for a high input frequency of 200 MHz. The clock generation is more complex than for a basic switched capacitor circuit, but it was found in the measurements that the logic and the clock distribution themselves did not consume much power.

APPENDIX

The time domain output of the sampler can be obtained by convolving the input signal with the samplers input response

$$v_o(t) = \int_{-\infty}^{\infty} h(t-\tau)v_{\text{in}}(\tau)d\tau \tag{19}$$

where $h(\tau)$ is the impulse response of the sampler. Assuming that the sampling switch is completely opened at $t = 0$ we may write the output after sampling as

$$v_o(t=0) = \int_{-\infty}^{\infty} h(-\tau)v_{\text{in}}(\tau)d\tau. \tag{20}$$

From (20) we define the sampling function as

$$SF(\tau) = h(-\tau). \tag{21}$$

It is obvious that the time after the switch has opened does not affect the sample value. Combining the (20) and (21) we may write

$$v_o(t=0) = \int_{-\infty}^{0} SF(\tau)v_{\text{in}}(\tau). \tag{22}$$

From (22) we note that the output is a weighted average of all previous time values of the input signal where the weighting function is equal to the impulse response of the sampler with the time scale reversed.

Let us consider a case where the switch conductance changes linearly from an initial value of g_s to zero during the time interval $-t_f$ and 0. Then the output voltage is described with a set of ordinary differential equations

$$\begin{cases} C_s\dfrac{dv_o}{dt} = g_s(v_{\text{in}}(t) - v_o(t)), & t < -t_f \\ C_s\dfrac{dv_o}{dt} = -\dfrac{g_s}{t_f}t(v_{\text{in}}(t) - v_o(t)), & -t_f \le t < 0 \\ C_s\dfrac{dv_o}{dt} = 0, & t \ge 0. \end{cases} \tag{23}$$

The last differential equation in (23) merely states that the output voltage does not change after $t = 0$, which means that the sampling function $SF(\tau)$ in that region is zero. The output voltage v_o at $t = 0$ can be found from (23) as

$$v_o(t=0) = -\frac{g_s}{C_s t_f}\int_{-t_f}^{0} v_{in}(\tau)\tau e^{-(g_s/2C_s t_f)\tau^2}d\tau + \frac{g_s}{C_s}e^{(g_s t_f/2C_s)}\int_{-\infty}^{-t_f} v_{in}(\tau)e^{(g_s C_s)\tau}d\tau. \tag{24}$$

Comparing (22) and (24), we find the sampling function as

$$\begin{cases} SF(\tau) = \dfrac{g_s}{C_s}e^{(g_s/C_s)((t_f/2)+\tau)}, & \tau < -t_f \\ SF(\tau) = -\dfrac{g_s}{C_s}\dfrac{\tau}{t_f}e^{-(g_s/2C_s t_f)\tau^2}, & -t_f \le \tau < 0. \end{cases} \tag{25}$$

Let us define the sampling aperture as the width of a rectangular sampling function with a height equal to the maximum of the actual sampling function. Assuming no loss at dc, the area of the sampling function $SF(\tau)$ is 1. Given this, it suffices to find the maximum of the sampling function and invert it to find the aperture. The maximum of (25) is always located between $-t_f$ and 0, because below $-t_f$ the function is monotonically increasing. Derivating the expression for $SF(\tau)$ after $-t_f$ and setting the derivative to zero we find a candidate for the sampling function maximum. However, as the function is discontinuous, the maximum may also be located at the border of the two regions or at $-t_f$. The two different cases for the location of the maximum are given by

$$\tau = \begin{cases} -\sqrt{\dfrac{C_s}{g_s}}t_f, & t_f > \dfrac{C_s}{g_s} \\ -t_f, & t_f \le \dfrac{C_s}{g_s}. \end{cases} \tag{26}$$

Substituting this into the sampling function and inverting we get the sampling aperture in two different regions as

$$a_t = \begin{cases} \sqrt{\tau_s t_f e}, & t_f > \dfrac{C_s}{g_s} \\ \tau_s e^{1/2t_f/\tau_s}, & t_f \le \dfrac{C_s}{g_s} \end{cases} \tag{27}$$

where τ_s is the switch *RC*-time constant C_s/g_s.

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